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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/342,235	06/29/1999	YASUHIKO TAKEMURA	0756-1980ELE	6257

7590

10/23/2002

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2010 CORPORATE RIDGE, SUITE 600  
MCLEAN, VA 22102

EXAMINER

SEFFER, AHMED N

ART UNIT

PAPER NUMBER

2814

DATE MAILED: 10/23/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

09/342,235

Applicant(s)

TAKEMURA, YASUHIKO

Examiner

A. Sefer

Art Unit

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☐ Responsive to communication(s) filed on 02 August 2002.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☐ Claim(s) 6-11 and 13-25 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) 6-11 is/are allowed.
- 6) ☐ Claim(s) 13-25 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

## Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 6, 10, 14 6) ☐ Other \_\_\_\_\_

## DETAILED ACTION

### *Response to Amendment*

1. The amendment filed on 8/02/02 has been entered. Claims 1-5 and 12 have been cancelled and new claims 25 and 25 have been added.

### *Claim Rejections - 35 USC § 102*

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

3. Claims 13-25 are rejected under 35 U.S.C. 102(e) as being anticipated by Yamazaki et al. US PG-Pub No.n2002/0090770.

Yamazaki et al disclose in figs. 4-6 a semiconductor device comprising a substrate having an insulating surface; at least first and second semiconductor islands formed over said substrate wherein each of the semiconductor islands has a channel region and a pair of impurity regions 603, 604/611, 612; a first and a second gate

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insulating film formed over said semiconductor island, respectively; at least first and second gate electrodes 605, 616 formed over said first and second semiconductor islands respectively with said first and second gate insulating films interposed therebetween; an interlayer insulating film 407 formed over a wiring (as in claims 16 and 19); a smoothing film 407 formed over a wiring (as in claims 20 and 23); a wiring for electrically connecting one of the impurity regions of the first semiconductor islands with the second gate electrode; and a pixel electrode electrically connected to one of the pair of the impurity regions of the second semiconductor island; or a pixel electrode 409 formed over said interlayer insulating film (as in claim 16) or a pixel electrode formed over said smoothing film (as in claim 20); wherein the first semiconductor island is a part of an NTFT and the second semiconductor island is a part of a PTFT.

As to claims 14, 17 and 21, Yamazaki et al disclose (see para. 0002) at least first and second semiconductor islands comprising polysilicon.

As to claims 15, 18 and 22, Yamazaki et al disclose a data line 408 electrically connected to the other one of the impurity region of the first semiconductor island.

As to claims 24 and 25, Yamazaki et al disclose in fig. 6B a voltage supply line  $V_d$  electrically connected to an impurity region of a semiconductor island.

***Allowable Subject Matter***

4. Claims 6-11 are allowed.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to A. Sefer whose telephone number is (703) 605-1227.

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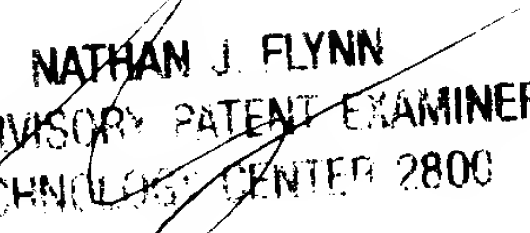
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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on (703) 308-6601.

ANS

October 20, 2002

  
NATHAN J. FLYNN  
SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER 2800